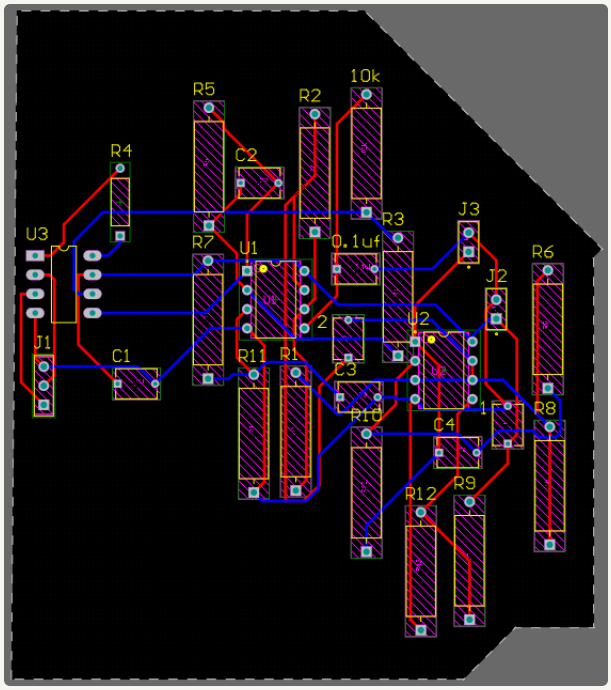
ENTRY 01 / PROJECT OVERVIEW

From microvolts to a heartbeat

Monday, November 24, 2026 | Lab 9 final project: ECG signal-conditioning circuit, schematic to fabrication-ready PCB in Altium

TODAY'S MILESTONE

Took the three-stage ECG signal-conditioning circuit from the lab's reference schematic to a validated, 100% routed, through-hole PCB with Gerber and drill files ready for fabrication.



The finished two-layer board after autorouting: 54 of 54 connections, red = top copper, blue = bottom copper. Input enters at J1 (left); power and output leave at J2/J3 (right).

What I set out to do

Turn the Lab 9 breadboard circuit (an AD623 instrumentation amplifier followed by two TLV2462 op-amp filter stages) into my own PCB, powered from the Feather's single 3.3 V rail. Because I am assembling the board myself, every part had to be through-hole and every connection to the outside world had to land on a real pad.

What actually happened

Most of the work was not drawing the circuit but making Altium agree with what I meant. Early versions shorted the amplifier inputs through junction dots, used vault parts that were secretly surface-mount, wired decoupling capacitors in series with the supply, and referenced a 1.65 V "virtual ground" that nothing was actually driving. Each problem was found by reading the schematic carefully or by the validator, and fixed one at a time.

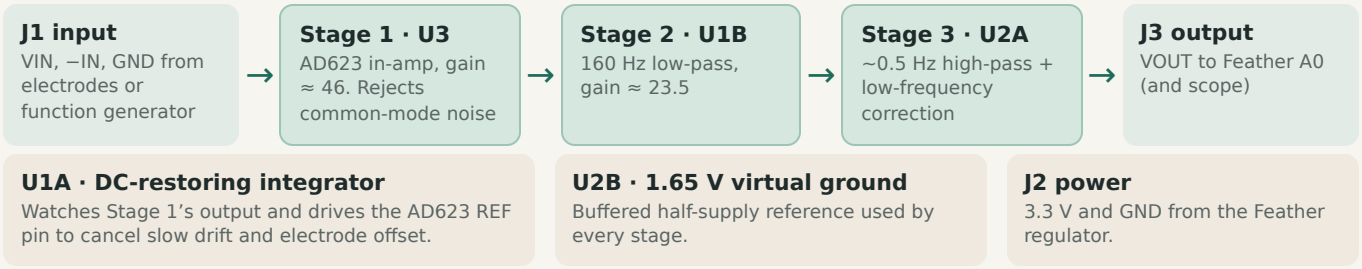
How the session ended

The schematic compiles with no errors, the PCB passes every electrical design-rule check (0 clearance, short-circuit, width and unrouted violations), and the Gerbers are zipped. The biggest lesson: a label in a schematic is a promise, not a connection. A net named 1.65V does nothing until a circuit drives it, and a part name does not say what the footprint is.

ENTRY 02 / SYSTEM OVERVIEW

What the board does

A ~1 mV heart signal in; a ~1 V signal the Feather's ADC can read out.



Why it needs three stages

An ECG at the skin is only about 1 mV, rides on electrode offsets that can be hundreds of millivolts, and shares the wires with 60 Hz mains pickup. A single high-gain amplifier would saturate on the offset immediately. So the design splits the job: the instrumentation amplifier takes the *difference* between two electrodes (rejecting noise common to both), an integrator loop strips out the DC, and the following stages shape the bandwidth to roughly 0.5–160 Hz, which contains the PQRST waveform, before adding the rest of the gain.

Why a virtual ground

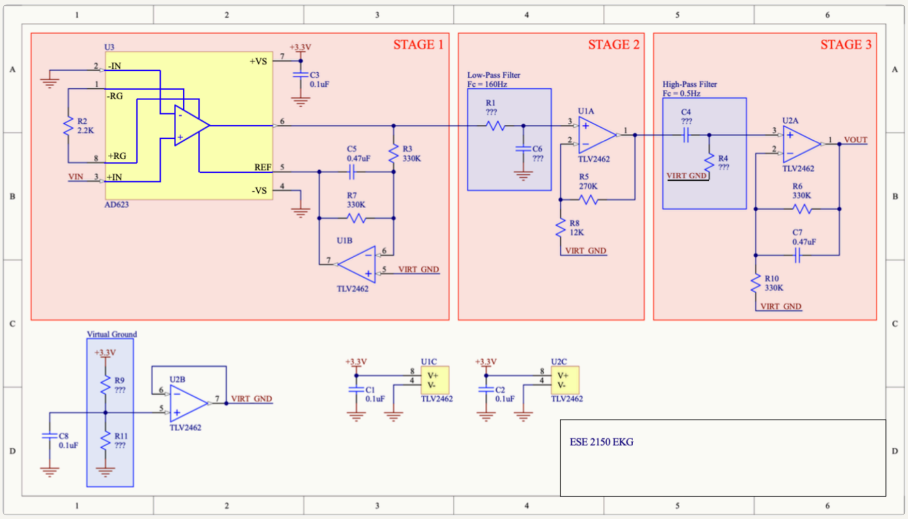
The board runs from one 3.3 V supply, so "zero" for an AC signal cannot be 0 V: the op-amps could not swing below it. Every stage is instead referenced to 1.65 V, the middle of the rail, which gives the largest symmetric swing. That reference must be **stiff**: it is a divider buffered by its own op-amp so that the resistors connected to it cannot pull it around.

PARAMETER	LAB TARGET	THIS BOARD (DESIGNED)	SET BY
Stage 1 gain	—	46.5× (33.3 dB)	R4 = 2.2 kΩ
Stage 2 gain	—	23.5× (27.4 dB)	R2 / R1 = 270k / 12k
Total mid-band gain	≈ 60 dB	≈ 1086× (60.7 dB)	all stages
Low-pass cutoff	160 Hz	159 Hz	10 kΩ · 0.1 µF
High-pass cutoff	0.5 Hz	0.53 Hz (overall −3 dB)	Stage 1 loop + Stage 3
Supply / reference	3.3 V	3.3 V / 1.65 V	Feather; R9, R12, U2B

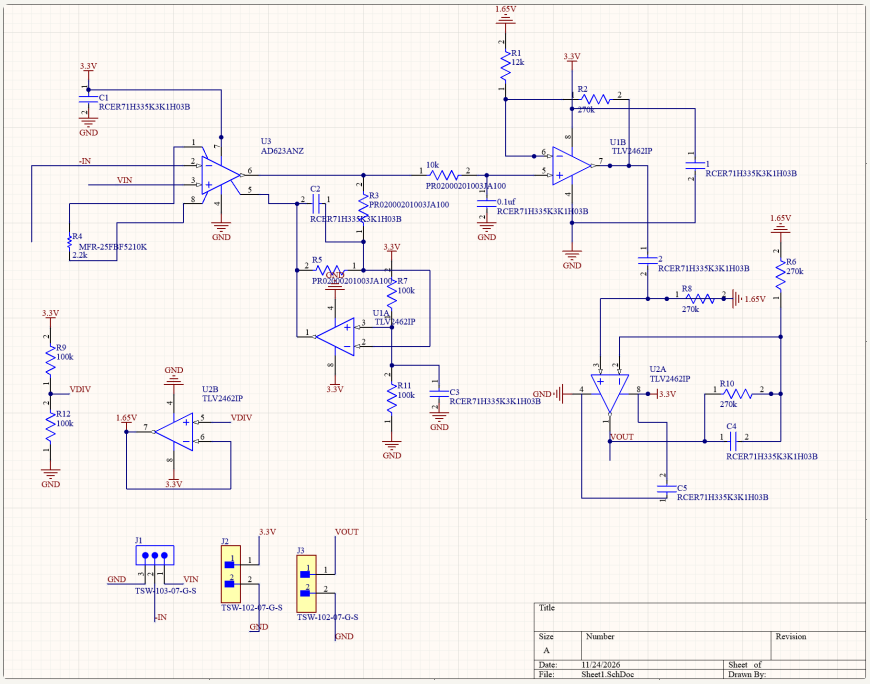
ENTRY 02 / SYSTEM OVERVIEW (CONT.)

From reference to my schematic

The lab's Figure 4 next to the schematic I drew in Altium.



Lab reference (Figure 4): three stages plus a virtual-ground block. Values marked ??? were left for the student to choose.



My final Altium schematic (ECG.SchDoc): Stage 1 left of centre, Stage 2 top right, Stage 3 bottom right, the 1.65 V divider and buffer bottom left, and connectors J1–J3 along the bottom edge.

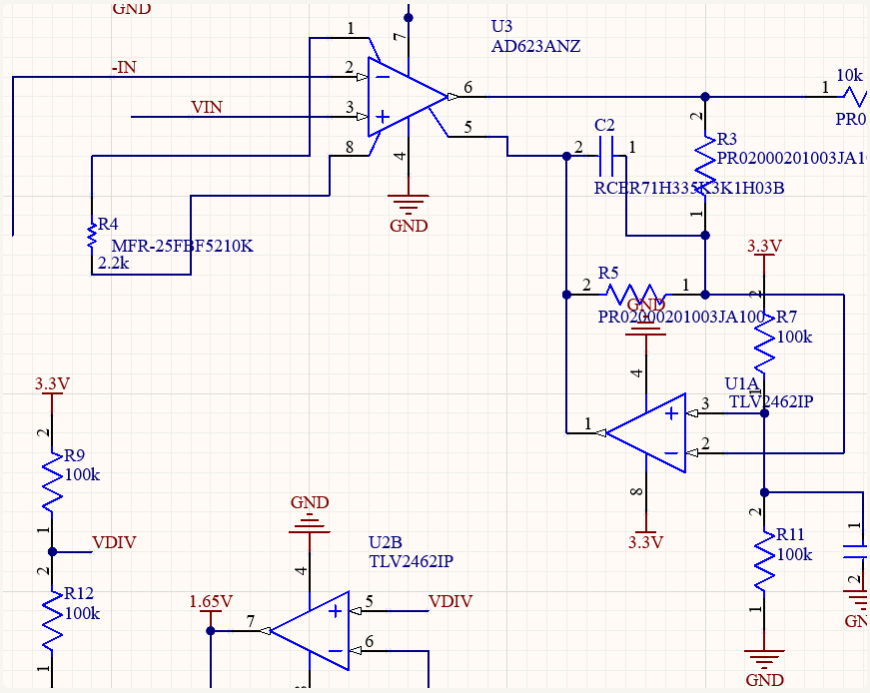
Where my design differs from Figure 4

- **−IN is not hard-wired to ground.** It runs to its own header pin, so one board can do both the grounded sine-wave test (add a jumper) and the two-electrode ECG test.
- **Component values come from parts I had on hand:** 100 kΩ / 3.3 µF in the integrator (lab: 330 kΩ / 0.47 µF) and 270 kΩ / 3.3 µF in Stage 3.
- **Op-amp halves are paired differently:** U1 = integrator (A) + Stage 2 (B); U2 = Stage 3 (A) + virtual-ground buffer (B).

ENTRY 03 / TECHNICAL NOTES · STAGE 1

The front end

AD623 instrumentation amplifier with a DC-restoring integrator on its REF pin.



Stage 1 in my schematic: U3 (AD623) with gain resistor R4 across pins 1/8; U1A integrator below, driving REF (pin 5).

AD623: amplify the difference, ignore the rest

The AD623 outputs the voltage *between* +IN and −IN times a gain set by one resistor, while rejecting anything that appears on both inputs equally, such as 60 Hz hum coupled into the body. Its output is not referenced to ground but to whatever voltage sits on its REF pin.

```
// AD623 gain, set by R4 between pins 1 and 8
G = 1 + 100 kΩ / R4 = 1 + 100 kΩ / 2.2 kΩ ≈ 46.5   (33.3 dB)
```

The integrator: a self-centring REF pin

U1A compares the AD623 output (through R3) with 1.65 V from the R7/R11 divider. Any slow drift away from 1.65 V gets integrated by C2 and fed back to REF in the opposite direction, pulling the output back to the centre. Fast signals like the heartbeat pass through. R5 across C2 keeps the loop “lossy”, so it attenuates very low frequencies by half rather than removing them completely; Stage 3 later undoes that dip.

```
// Stage 1 with the integrator loop (R3 = R5 = 100 kΩ, C2 = 3.3 µF, τ = 0.33 s)
H1(s) = G · (1 + sτ) / (2 + sτ)
// DC: G/2 ≈ 23    zero ≈ 0.48 Hz    pole ≈ 0.96 Hz    in-band: G ≈ 46.5
```

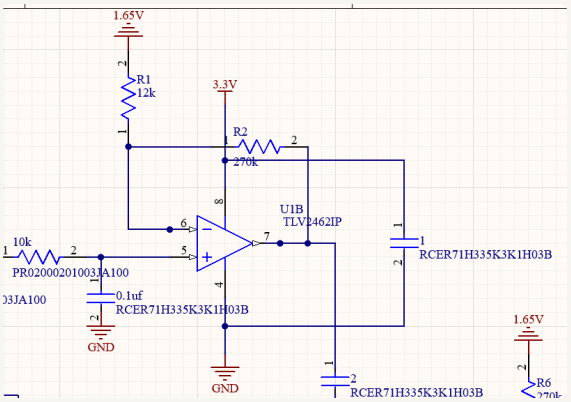
STAGE 1 PARTS

U3 AD623ANZ (DIP-8) • R4 2.2 kΩ gain • U1A TLV2462 integrator • R3, R5 100 kΩ • C2 3.3 µF • R7/R11 100 kΩ divider + C3 filter • C1 decoupling on pin 7

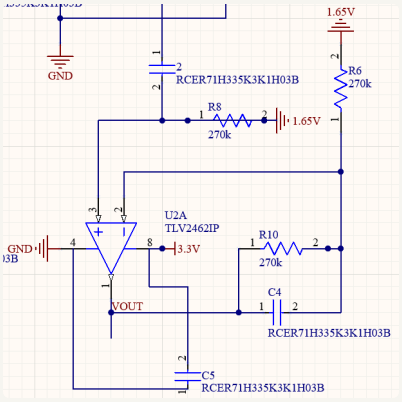
ENTRY 03 / TECHNICAL NOTES · STAGES 2, 3 AND THE REFERENCE

Shaping the band

A 160 Hz low-pass with gain, a 0.5 Hz high-pass with correction, and the 1.65 V reference both depend on.



Stage 2 (U1B): RC low-pass into a non-inverting gain stage.



Stage 3 (U2A): high-pass at the + input, R10 ‖ C4 feedback.

Stage 2: remove what isn’t heart

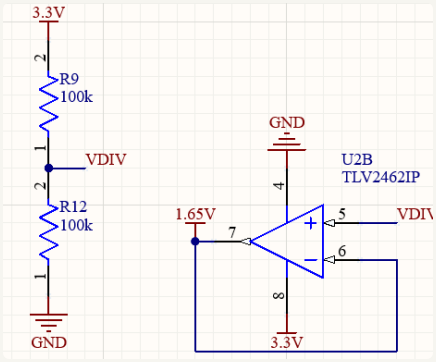
The 10 kΩ / 0.1 µF RC at U1B’s + input rolls off everything above 159 Hz, trimming high-frequency noise, before more gain is added. U1B is then a non-inverting amplifier referenced to 1.65 V: R1 goes to the virtual ground, not to 0 V, so the 1.65 V bias is not multiplied along with the signal.

```
f_c = 1 / (2π · 10 kΩ · 0.1 µF) ≈ 159 Hz        G2 = 1 + R2/R1 = 1 + 270k/12k = 23.5
```

Stage 3: block DC, then correct the low end

A series capacitor with R8 to 1.65 V forms the high-pass, stripping any DC left after Stage 2. The feedback network R10 ‖ C4 with R6 to 1.65 V gives a gain of 2 at very low frequency and 1 in-band: a deliberate boost that compensates for the 6 dB dip created by Stage 1’s lossy integrator.

```
HPF: f = 1 / (2π · 270 kΩ · 3.3 µF) ≈ 0.18 Hz    correction: (2 + sτ)/(1 + sτ), τ = 0.89 s
```



Virtual ground: R9/R12 divider → VDIV → U2B follower → 1.65V net.

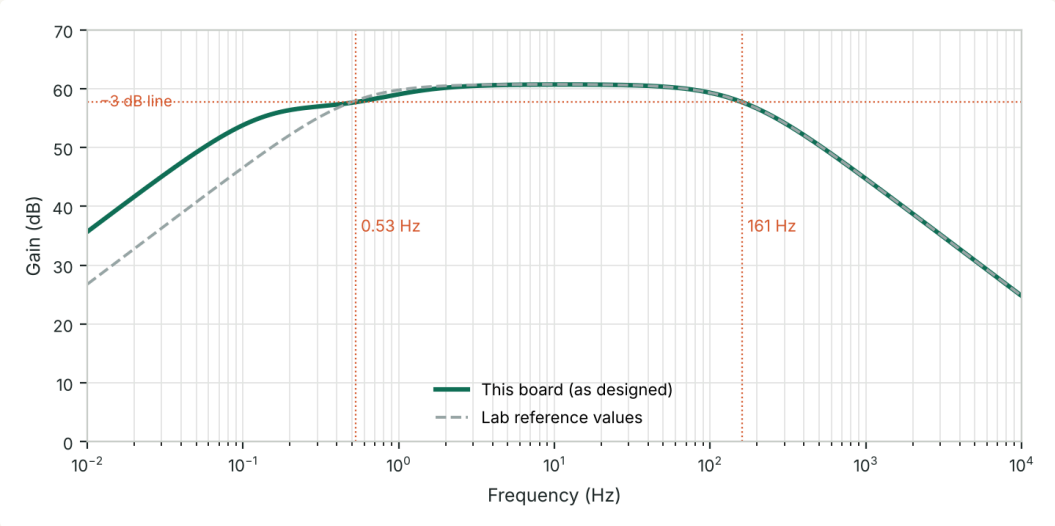
The 1.65 V reference

Two 100 kΩ resistors split 3.3 V in half. On its own that point is weak: every resistor tied to it would drag it around. U2B, wired as a voltage follower (output tied to its own − input), copies 1.65 V onto a low-impedance net. In Altium, every power port named `1.65V` joins that net by name.

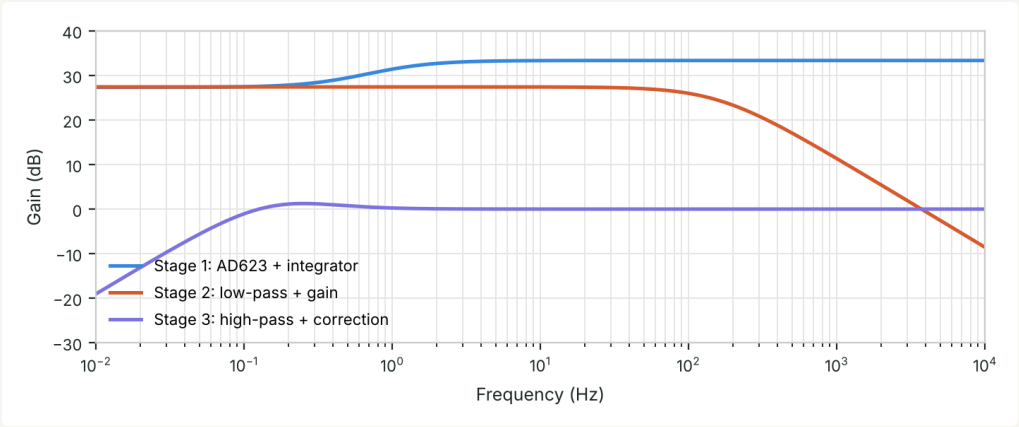
ENTRY 04 / PREDICTED RESPONSE

What the numbers say

Frequency response calculated from the component values on the board, using ideal op-amps.



Overall gain of the three stages in cascade. My values (solid) land on nearly the same passband as the lab's reference values (dashed): ~60.7 dB peak, −3 dB at 0.53 Hz and 160 Hz.



Each stage alone. Stage 1's low-frequency dip (blue) and Stage 3's correction boost (purple) partly cancel; Stage 2 (orange) sets the upper edge.

FREQUENCY	PREDICTED GAIN	LAB CHECKPOINT
0.5 Hz	57.6 dB (761×)	HPF corner: output should be ~70% of mid-band
10 Hz	60.7 dB (1086×)	Mid-band maximum
100 Hz	59.3 dB (924×)	Test-signal frequency
160 Hz	57.7 dB (770×)	LPF corner: output should be ~70% of max
1 kHz	44.7 dB (172×)	Upper end of the Bode sweep

PREDICTED, NOT YET MEASURED

A 2 mVpp, 100 Hz test signal should come out at about **1.85 Vpp** centred on 1.65 V, inside the 0–3.3 V rails with roughly 0.7 V of headroom. A larger input will clip. These numbers come from the schematic values; the bench measurements in the lab procedure will confirm or correct them.

ENTRY 05 / DEBUGGING RECORD

Making Altium mean what I meant

A step-by-step record of what was found wrong in the schematic, and how each issue was fixed.

01 **Junction dots shorted the inputs**
One vertical wire from pin 3 down to the VIN port picked up junction dots where it crossed pins 2, 1 and 8. That merged +IN, −IN, both gain pins and GND into one net, which is why Vin kept reporting as “GND”. Rewired so wires cross without junctions.

02 **Labels don’t make pads**
Ports and power ports name nets but create no copper. Replaced the floating VIN/−IN arrows with net labels tied to real THT pin headers: J1 (input), J2 (power), J3 (output).

03 **“Through-hole” parts that weren’t**
AD623**B**RZ and TLV2462**ID**G4 are SOIC packages. Switched to AD623ANZ / TLV2462IP. The vault AD623 was locked to SOIC footprints, so I copied it into my own library and built a DIP-8 footprint with the Footprint Wizard (page 8).

04 **Integrator wired as positive feedback**
The R/C node first went to the op-amp’s + input with − tied to GND, which would latch REF to a rail. Corrected to node → −, and + → 1.65 V rather than 0 V.

05 **Decoupling caps in series with the supply**
On the Stage 2 op-amp, 3.3 V went *through* a capacitor into pin 8, so the chip would have had no DC power. Rewired with pins straight to the rails and one cap across them.

06 **A reference with no source**
Several resistors pointed at a 1.65V port that nothing drove. Added the R9/R12 divider and the U2B follower, and labelled its output 1.65V. Also removed a 1.65V label accidentally placed on the integrator’s output.

07 **One chip, two op-amps**
Every triangle was “U?A”, which would have produced extra chips. Set designators and parts so the four op-amps live in two packages: U1A/U1B and U2A/U2B.

08 **Validator cleanup**
C5 touched U2’s power pins mid-pin, not at their tips (“net has only one pin”). The AD623’s REF pin was typed as a Power pin, flagging an Output-to-Power conflict that is intentional here. The remaining “no driving source” warnings are normal for nets driven by passives and headers.

VALIDATION / CAPTURED RESULTS

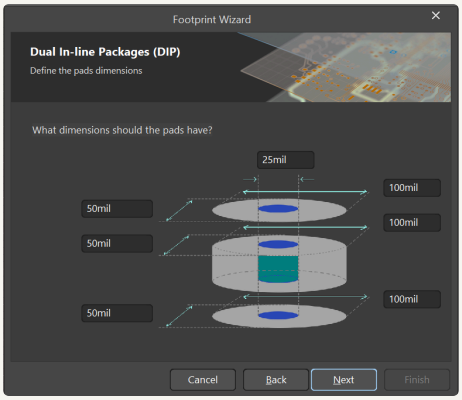
```
Project → Validate: Compile successful, no errors found
Situs autorouter: 54 of 54 connections routed — Routing finished
DRC: Clearance 0 | Short-circuit 0 | Un-routed 0 | Width 0 | Silkscreen 6
```

ENTRY 06 / FOOTPRINTS

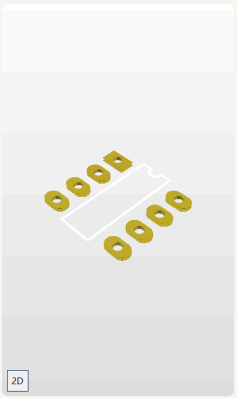
Building a DIP-8 footprint

Why the part name wasn’t enough, and how the AD623 became through-hole.

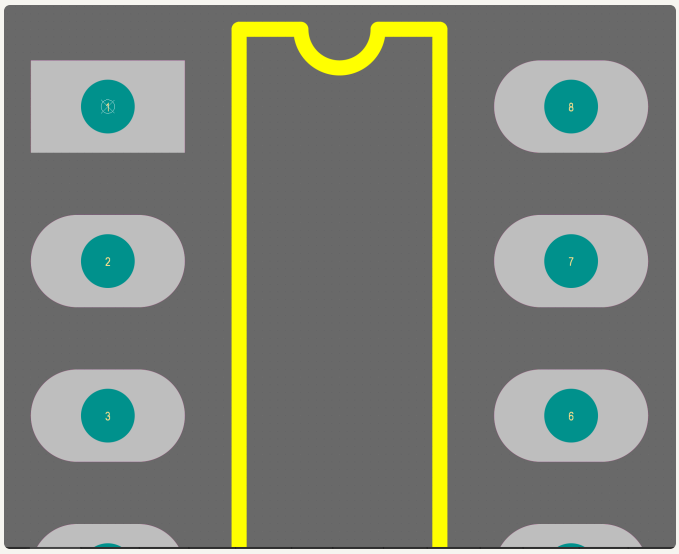
Changing a part’s comment to “AD623ANZ” only changes the label. The footprint, the copper pattern on the board, is what decides surface-mount versus through-hole, and the vault part was locked to three SOIC variants. The fix was a local copy: `Design → Make Schematic Library` for an editable symbol, a new `ECG.PcbLib`, and the Footprint Wizard’s dual in-line template.



Footprint Wizard: pad and hole dimensions for a dual in-line package.



3D preview of the new DIP8 footprint.



DIP8 in ECG.PcbLib: square pin 1 next to the notch, pins numbered counter-clockwise, every pad Multi-Layer (plated through-hole).

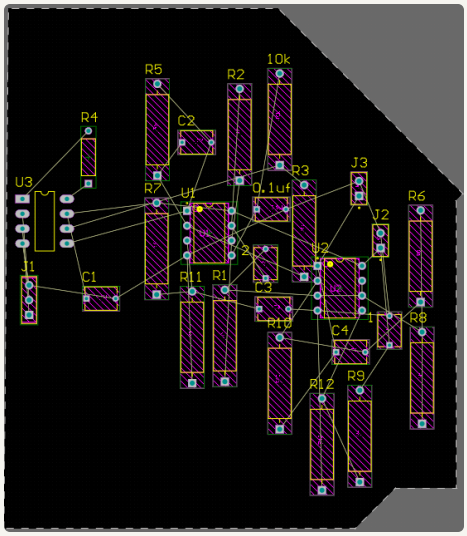
```
// DIP8 footprint settings
Pad: 60 × 100 mil oval   Hole: 35 mil (≈0.9 mm)   Pitch: 100 mil   Row spacing: 300 mil   Pads: 8
```

The pin numbering of the SOIC and DIP versions is identical, so the existing symbol kept working: only the attached footprint changed. On the board, a through-hole pad shows a hole size and sits on the Multi-Layer, which is a quick check for every part before routing.

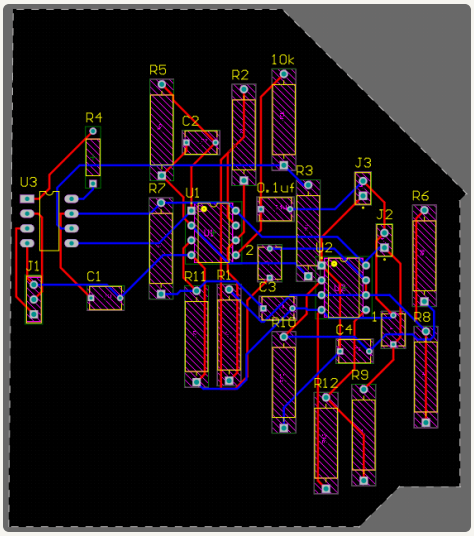
ENTRY 07 / LAYOUT & FABRICATION

From ratsnest to Gerbers

Placement, routing, design-rule check and fabrication outputs.



Placement: each chip clustered with its own parts. Thin lines are the ratsnest (connections still to route).

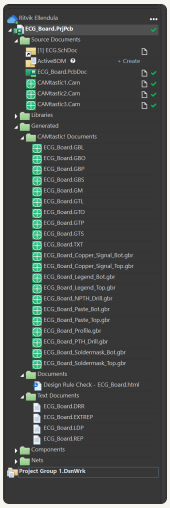


After autorouting with Situs: 100% routed on two layers.

Placement and rules

Parts were grouped by chip in signal order (U3 → U1 → U2), with the input header on one side, away from the output, and the board outline redrawn to fit. Rules were set generously for home fabrication: traces 15–30 mil (20 preferred) and 14 mil minimum clearance.

DRC CHECK	RESULT	NOTE
Clearance · Short-circuit · Un-routed · Width	0 · 0 · 0 · 0	Electrically clean
Hole size · Hole-to-hole · Solder-mask sliver	0 · 0 · 0	—
Silk-to-solder-mask / Silk-to-silk	3 / 3	Cosmetic: C3, R10, U2 labels overlap outlines



Generated outputs in the project.

Fabrication files

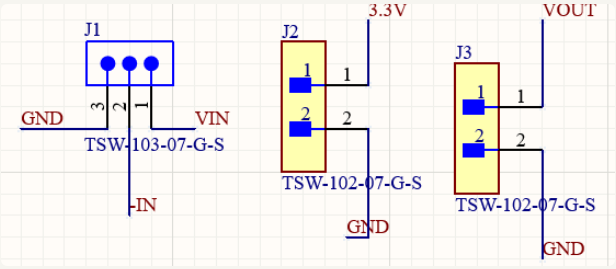
FILE	LAYER
.GTL / .GBL	Top / bottom copper
.GTS / .GBS	Top / bottom solder mask
.GTO / .GBO	Top / bottom silkscreen
.GM	Board outline
.TXT	NC drill (hole positions)

Exported as classic RS-274X files, with an X2 .gbr set generated alongside, then zipped for fabrication.

ENTRY 08 / DESIGN REVIEW & REFLECTION

Before the board is powered

Open items, the bench plan, and what I’d carry into the next design.



Off-board connections: J1 input (VIN, −IN, GND), J2 power (3.3 V, GND), J3 output (VOUT, GND).

Connector pinout

HEADER	PIN 1	PIN 2	PIN 3
J1 input	VIN	−IN	GND
J2 power	3.3 V	GND	—
J3 output	VOUT	GND	—

Open items found in review

☐ **C5 (U2 decoupling) is on the schematic but did not reach the PCB.** Re-run Update PCB, place it beside U2 pins 8 and 4, and re-export.

☐ **Designators:** four parts were annotated as “1”, “2”, “0.1uf” and “10k”. Rename them to C6, C7, C8 and R13.

☐ **BOM part numbers disagree with values:** the 10 kΩ, the 0.1 µF and the 2.2 kΩ show 100 kΩ, 3.3 µF and 10 kΩ part numbers. Solder what the values say.

☐ Silkscreen overlaps on C3, R10 and U2; a leftover wire stub on −IN.

Next bench session / not yet completed

☐ Fabricate and assemble; check pin 1 orientation on U1, U2 and U3.

☐ Power from the Feather; confirm 1.65 V at the buffer output before applying a signal.

☐ 2 mVpp, 100 Hz into J1 (−IN jumpered to GND); probe each stage; expect ~1.85 Vpp at VOUT.

☐ Bode sweeps 10 Hz–1 kHz; verify 160 Hz and 0.5 Hz corners; then the ECG simulator and Feather ADC.

REFLECTION

I now treat a schematic as two separate claims: what is *connected* (wires, labels, pin tips) and what is *physical* (footprints, headers, decoupling placement). Most of my bugs lived in the gap between them. Checking connectivity with the validator, and physicality by inspecting pads on the board, caught problems that looked fine on the drawing.